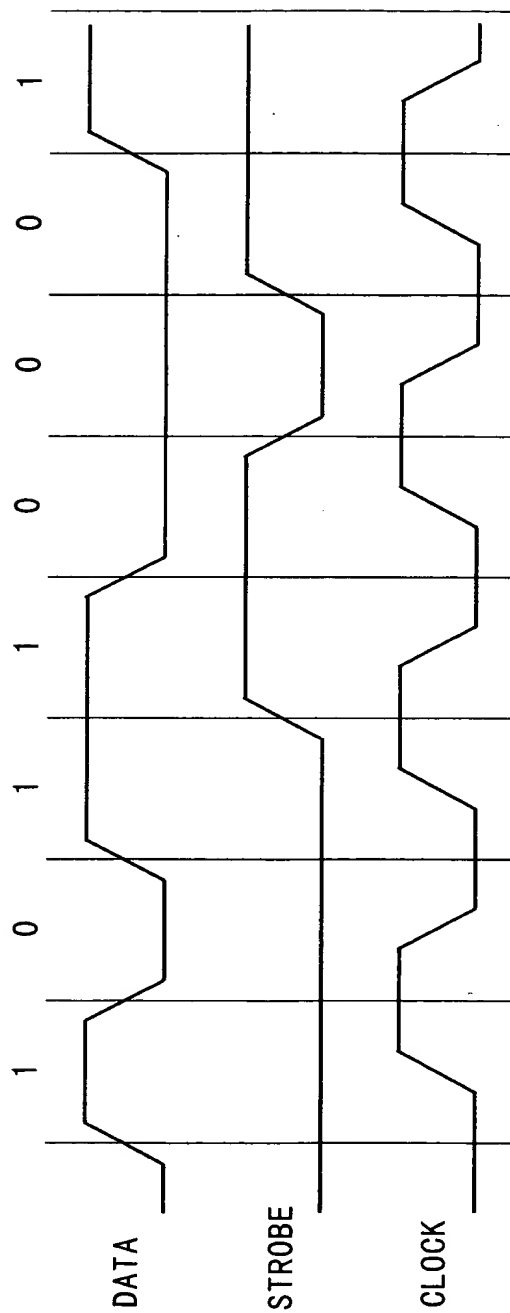


105070" FBZ2860

FIG. 1



00\*\*9556\*\*00

0327841-040501  
105070 "14B/2360

FIG. 2

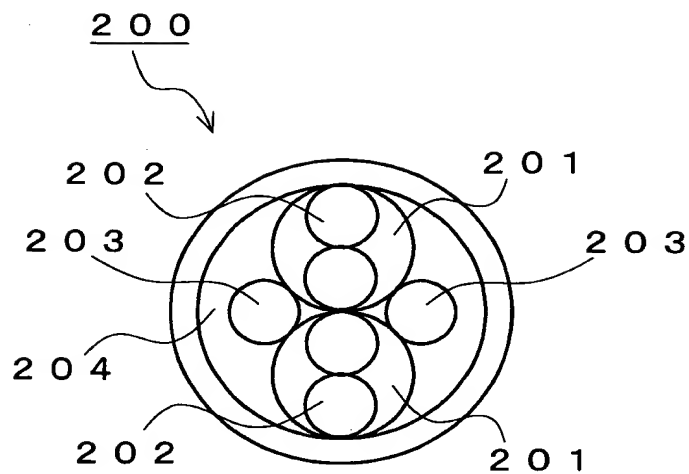
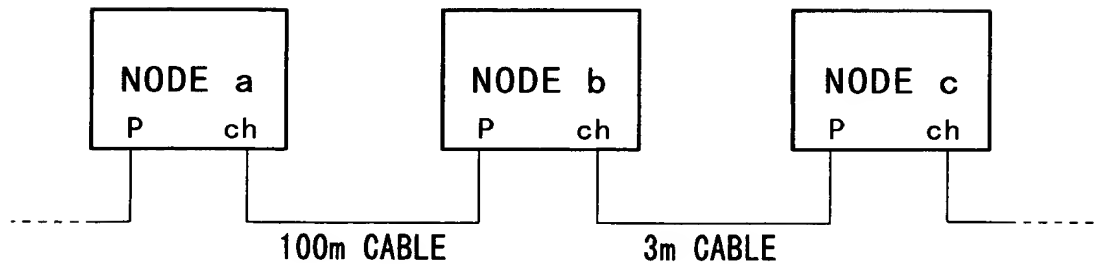


FIG. 5



09827841 040501  
105040 14822850

FIG. 3A  
(BUS INITIALIZATION)

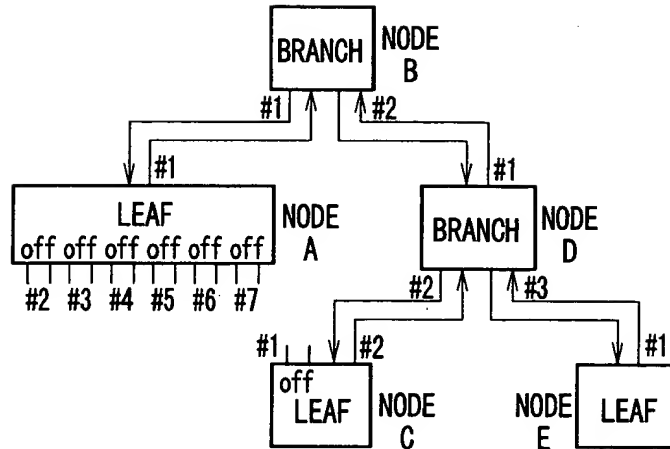


FIG. 3B  
(TREE IDENTIFICATION)

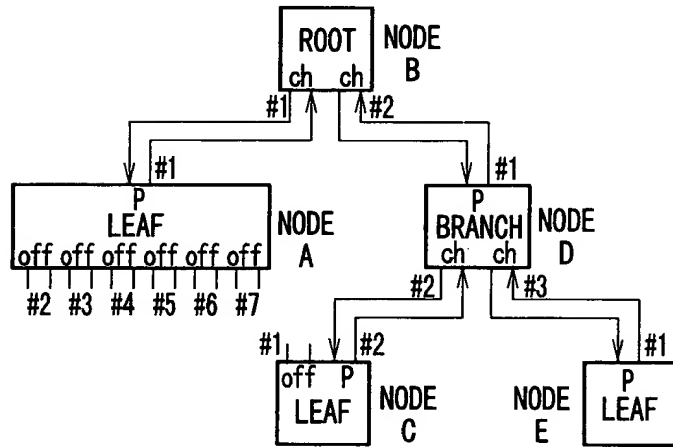


FIG. 3C  
(SELF IDENTIFICATION)

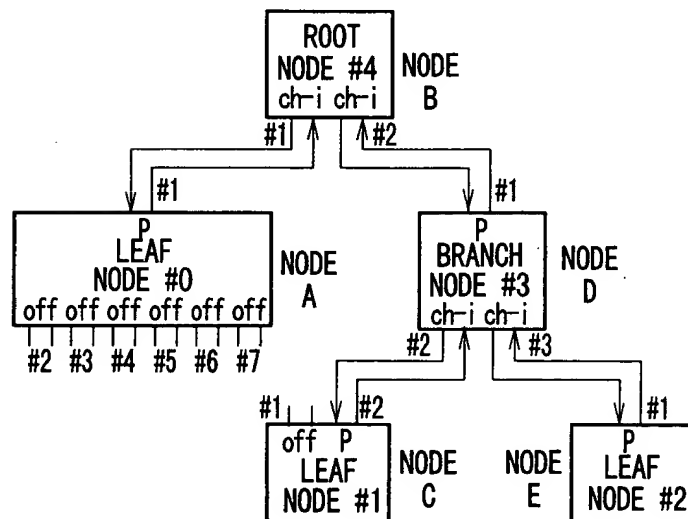


FIG. 4

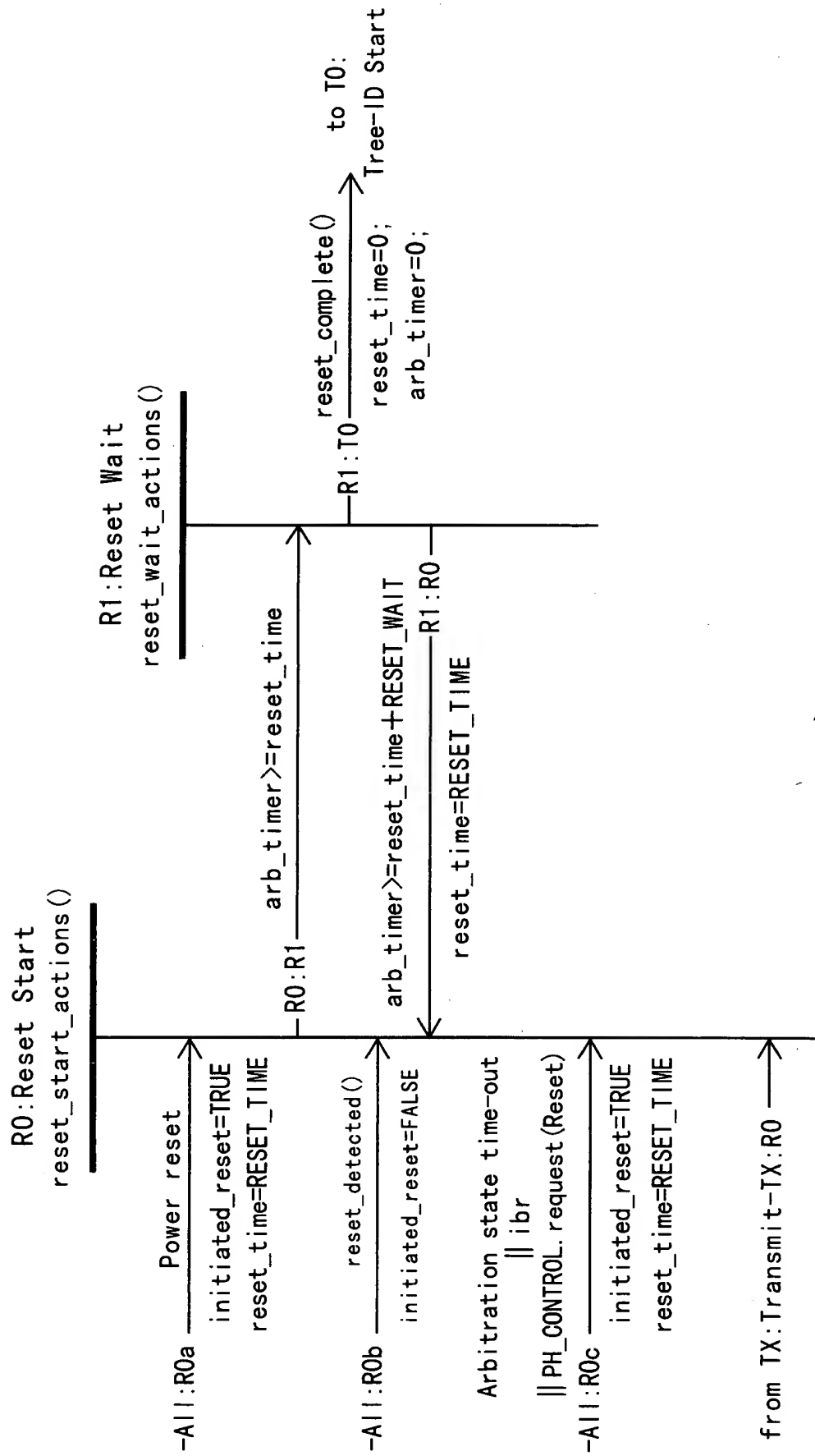


FIG. 6

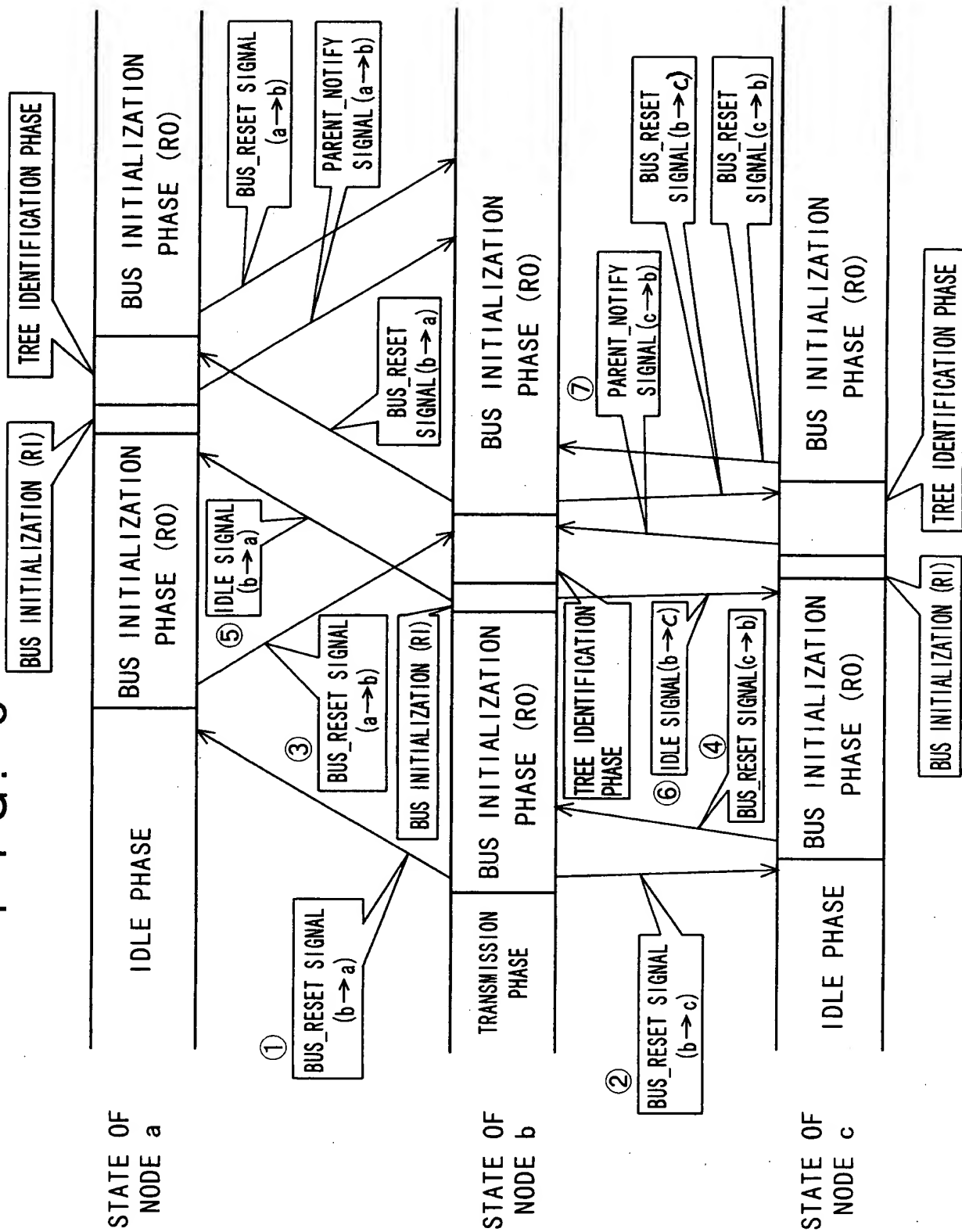


FIG. 7

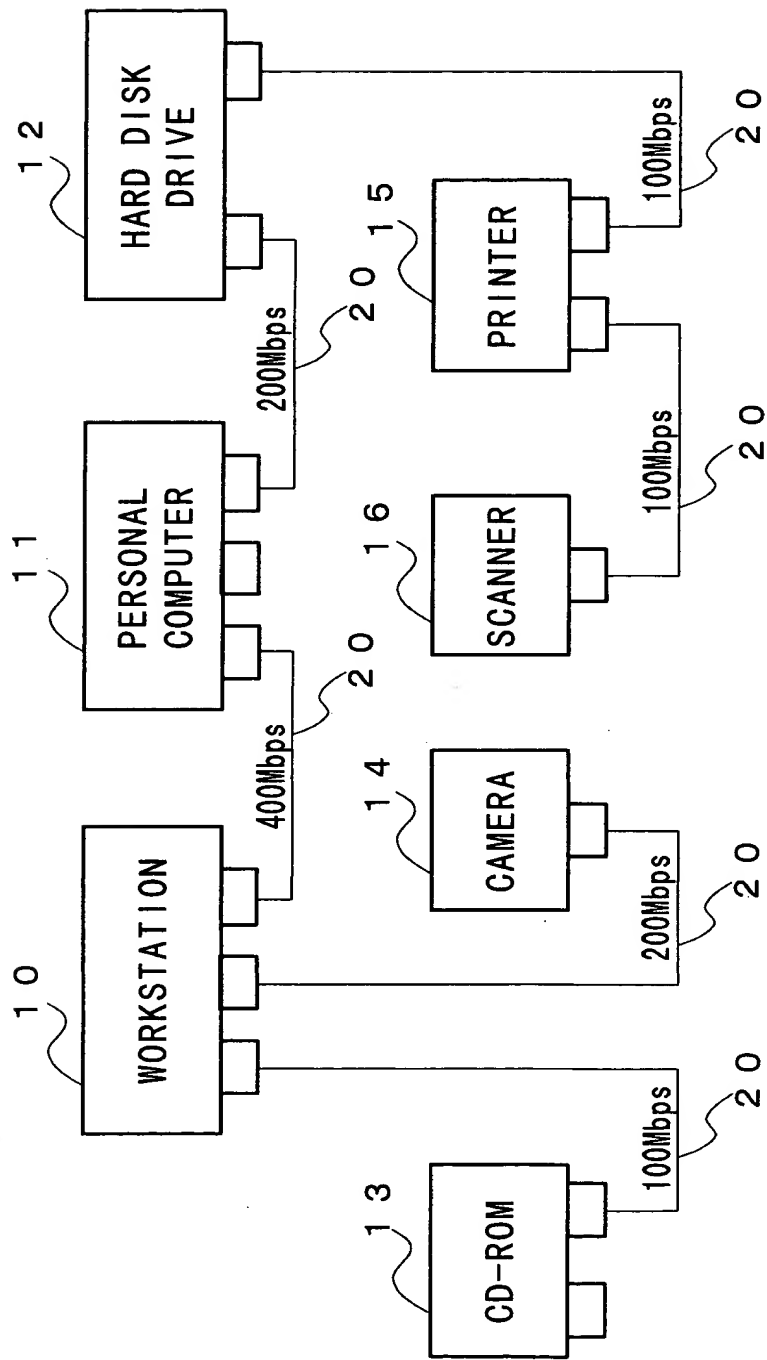


FIG. 8

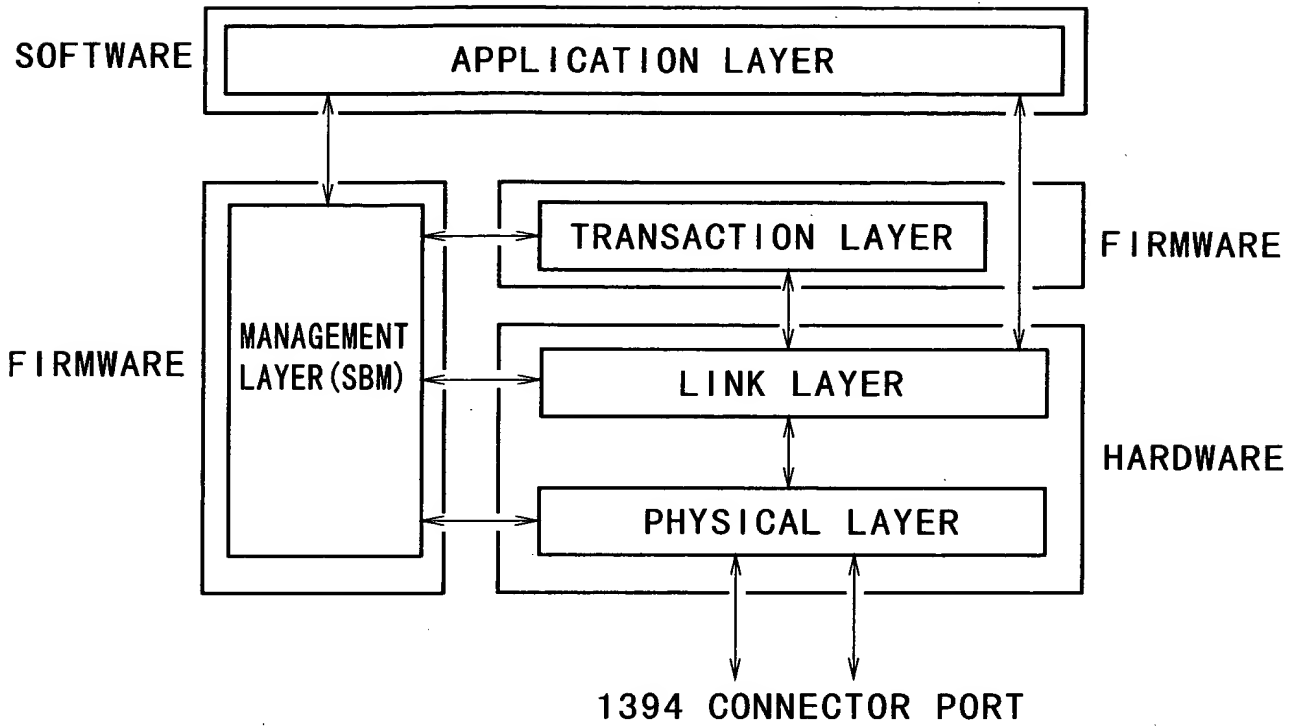


FIG. 9



FIG. 10A

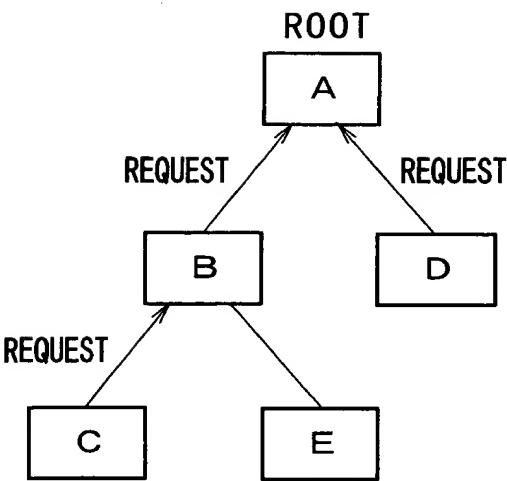


FIG. 10B

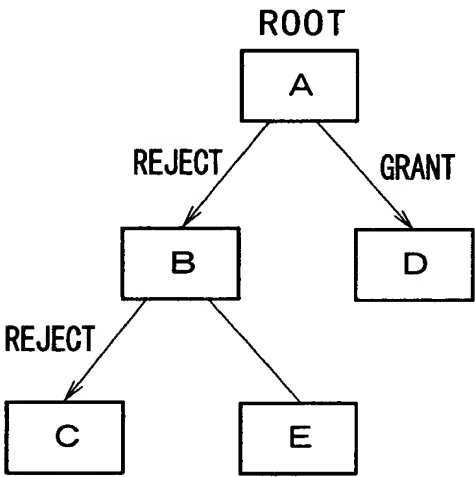


FIG. 11

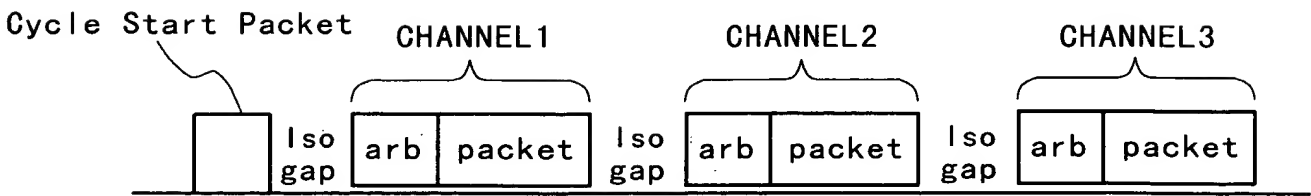
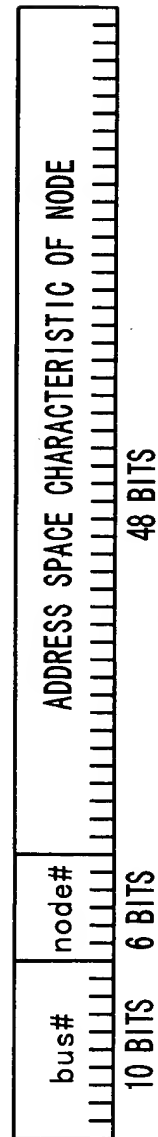
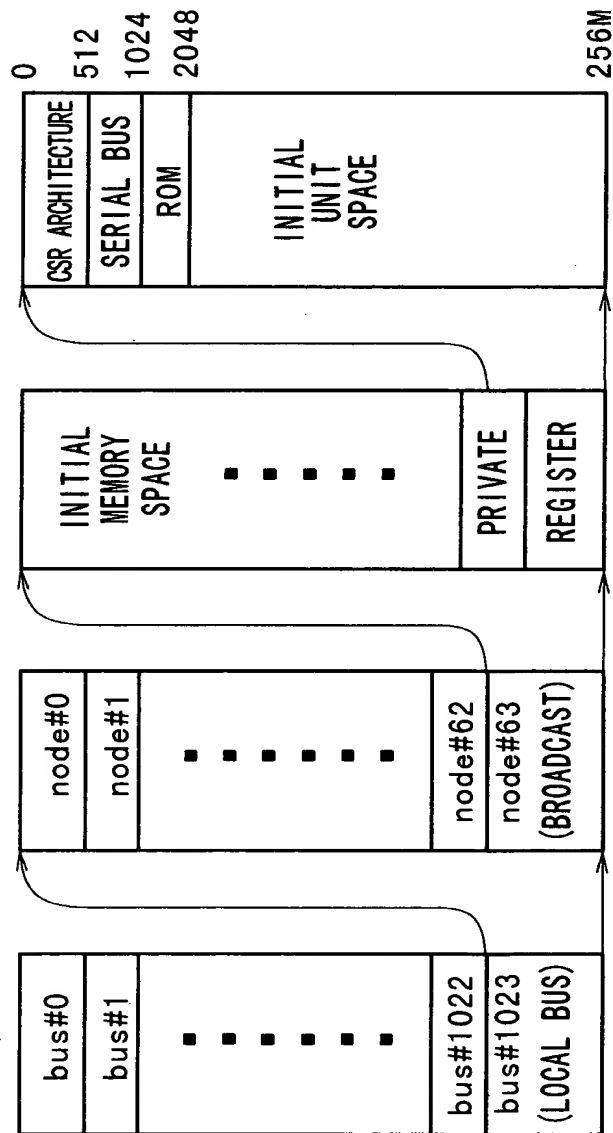


FIG. 12



F I G. 1 3

OFFSETS	NAMES	FUNCTIONS
000h	STATE_CLEAR	STATE AND CONTROL INFORMATION
004h	STATE_SET	SET STATE_CLEAR BIT
008h	NODE_IDS	INDICATE 16-BIT NODE ID
00Ch	RESET_START	START COMMAND RESET
018h-01Ch	SPLIT_TIMEOUT	PRESCRIBE MAXIMUM TIME OF SPLIT
200h	CYCLE_TIME	CYCLE TIME
210h	BUSY_TIMEOUT	PRESCRIBE LIMIT OF RETRY
21Ch	BUS_MANAGER	INDICATE BUS MANAGER ID
220h	BANDWIDTH_AVAILABLE	INDICATE BANDWIDTH THAT CAN BE ASSIGNED TO ISOCHRONOUS COMMUNICATION
224h-228h	CHANNELS_AVAILABLE	INDICATE USED STATE OF EACH CHANNEL

FIG. 14

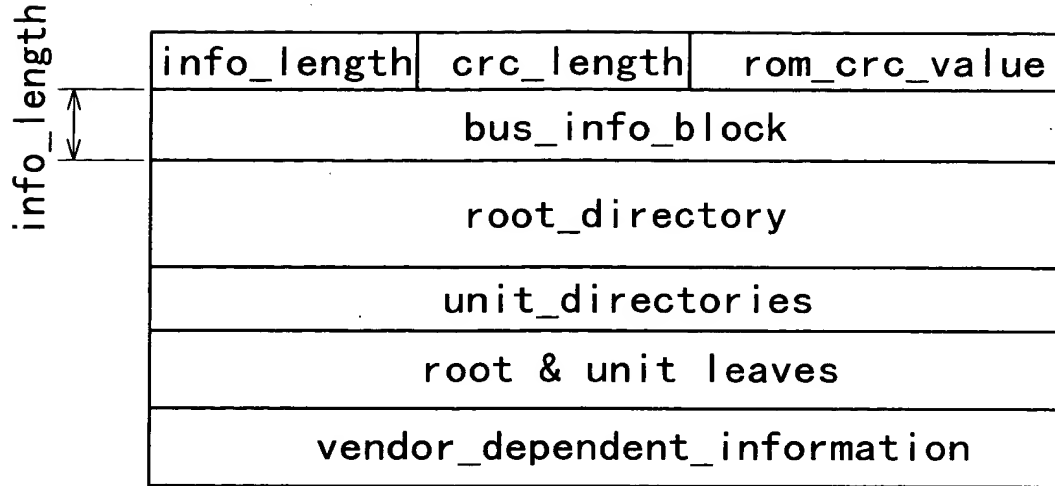


FIG. 16

900h	Output Master Plug Register
904h	Output Plug Control Register #0
908h	Output Plug Control Register #1
⋮	⋮
97Ch	Output Plug Control Register #30
980h	Input Master Plug Register
984h	Input Plug Control Register #0
988h	Input Plug Control Register #1
⋮	⋮
9FCh	Input Plug Control Register #30

# FIG. 15

400h	04h	crc_length	rom_crc_value
------	-----	------------	---------------

## Bus\_info\_block

404h	"1394"		
408h	img	img	img
40Ch	reserved	cyc_clk_acc	max_rec
410h	Company_ID		Chip_ID_hi
	Chip_ID_lo		

## Root\_directory

414h	root_length	CRC
418h	03h	module_vendor_id
41Ch	0Ch	node_capabilities
420h	8Dh	node_unique_id offset
424h	D1h	unit_directory_offset
428h	Optional.	

## Unit\_directory

unit_directory_length	CRC
12h	unit_spec_id
13h	unit_sw_version
Optional.	

FIG. 15 is a block diagram of a 1394 bus device.

FIG. 17A

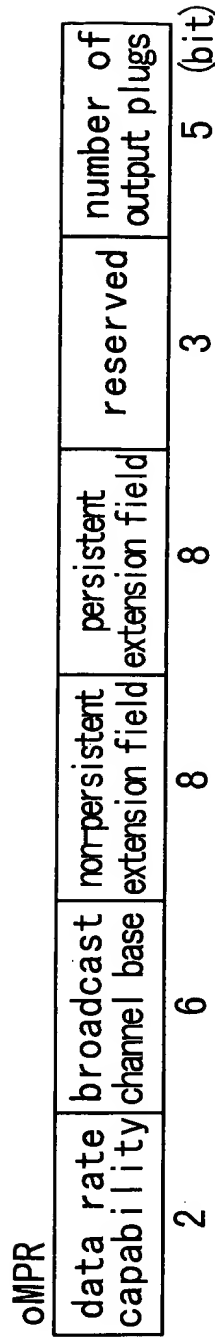


FIG. 17B

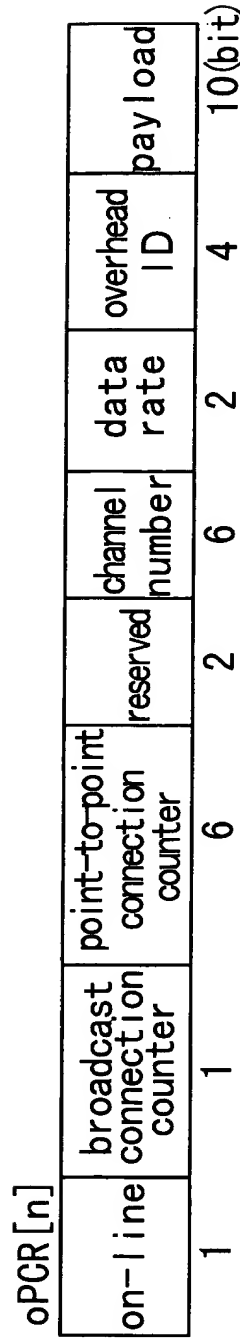


FIG. 17C

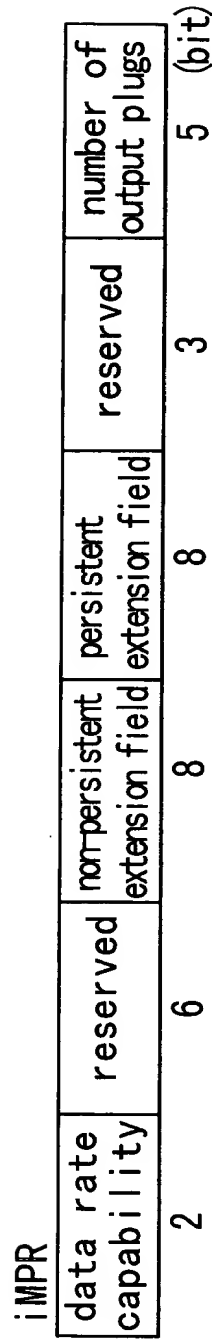


FIG. 17D

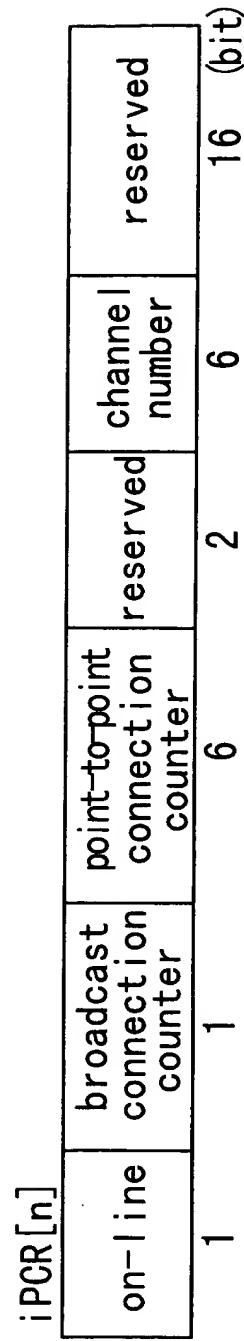


FIG. 18

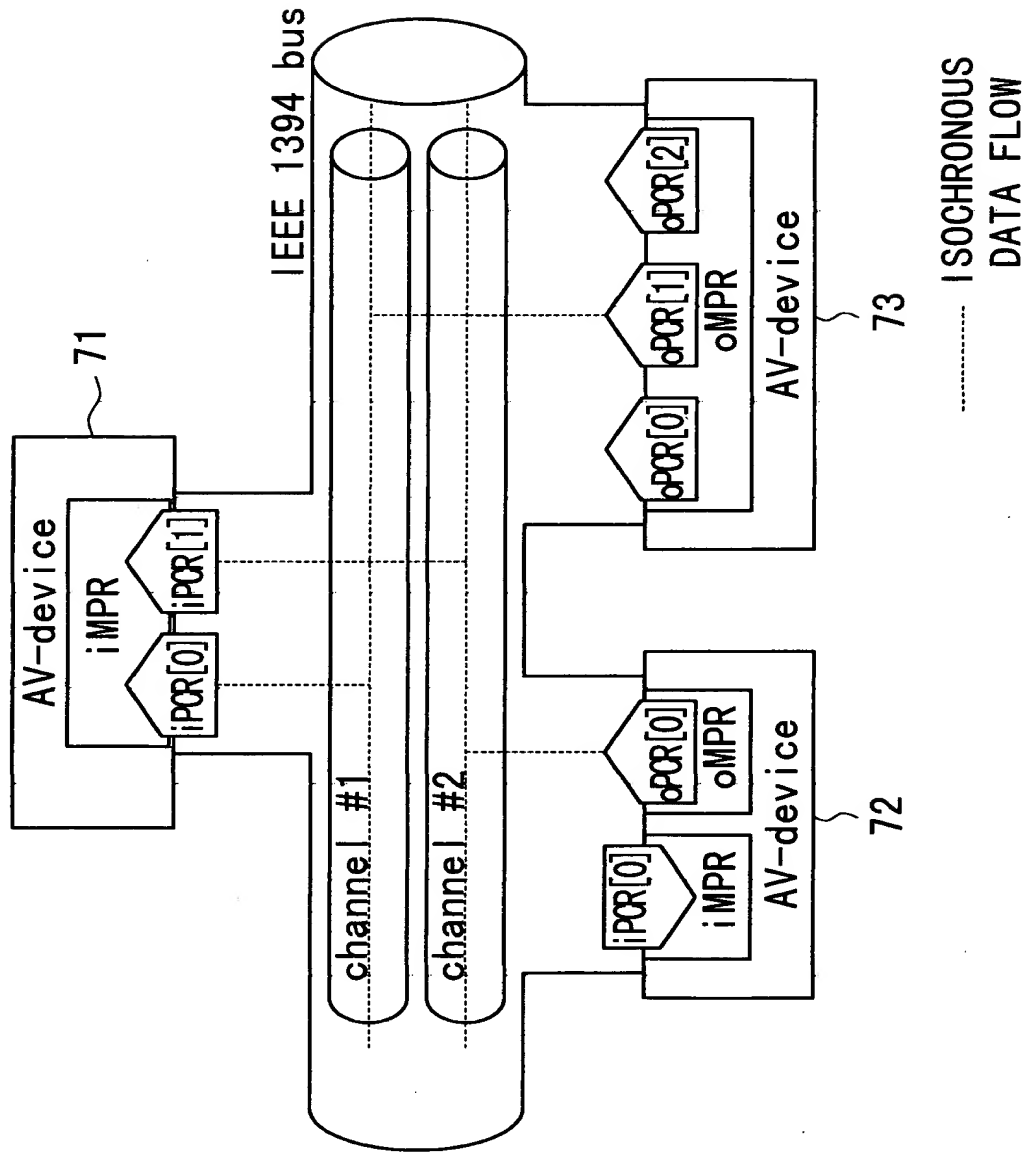
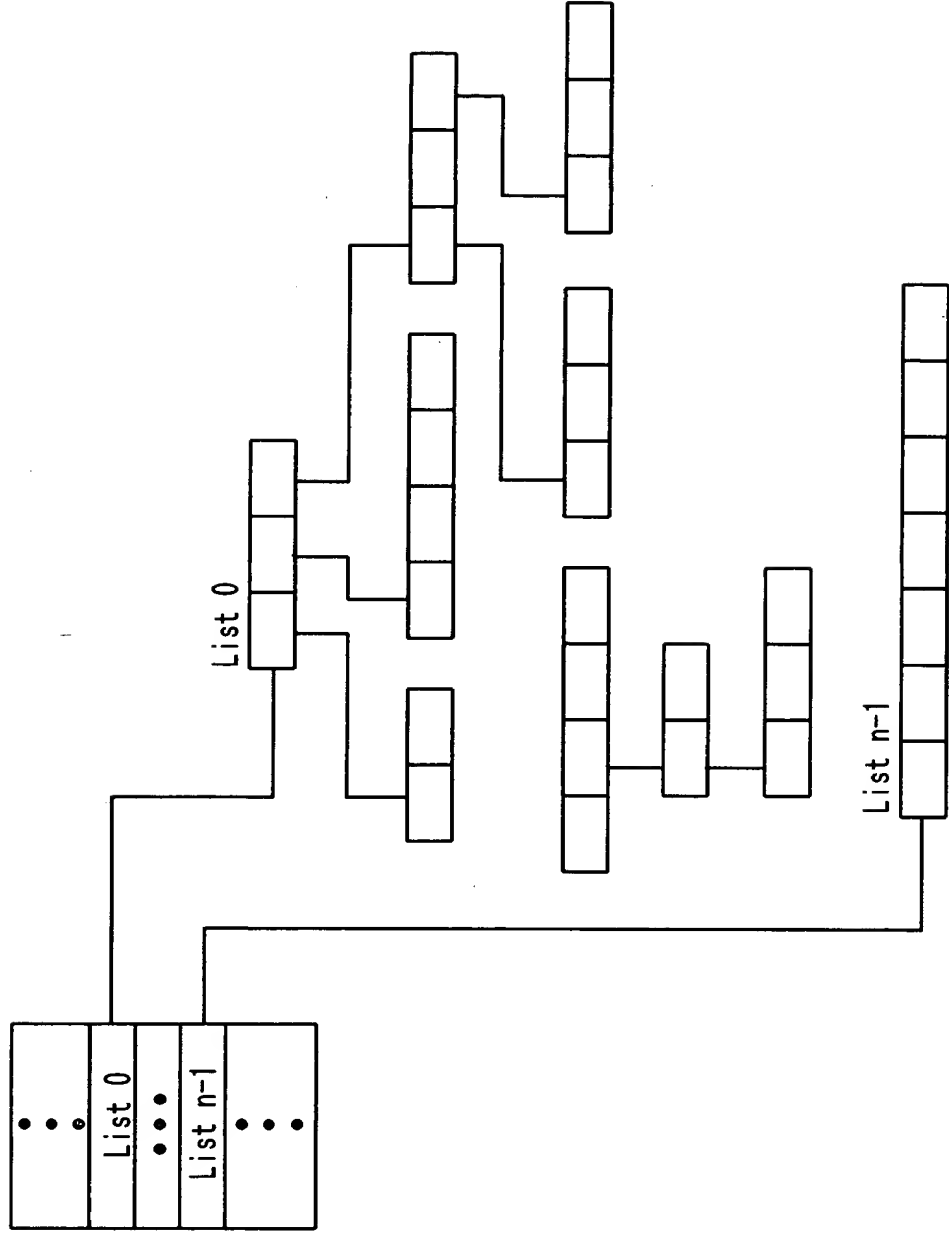


FIG. 19



# FIG. 20

The General Subunit Identifier Descriptor	
address	contents
00 00 <sub>16</sub>	descriptor_length
00 01 <sub>16</sub>	
00 02 <sub>16</sub>	generation_ID
00 03 <sub>16</sub>	size_of_list_ID
00 04 <sub>16</sub>	size_of_object_ID
00 05 <sub>16</sub>	size_of_object_position
00 06 <sub>16</sub>	number_of_root_object_lists(n)
00 07 <sub>16</sub>	
00 08 <sub>16</sub>	root_object_list_id_0
	root_object_list_id_n-1
	subunit_dependent_length
	subunit_dependent_information
	manufacturer_dependent_length
	manufacturer_dependent_information

09827844.040504  
105040.1482850

[illegible]

**00000000000000000000000000000000**

[illegible]

**00000000000000000000000000000000**

FIG. 23

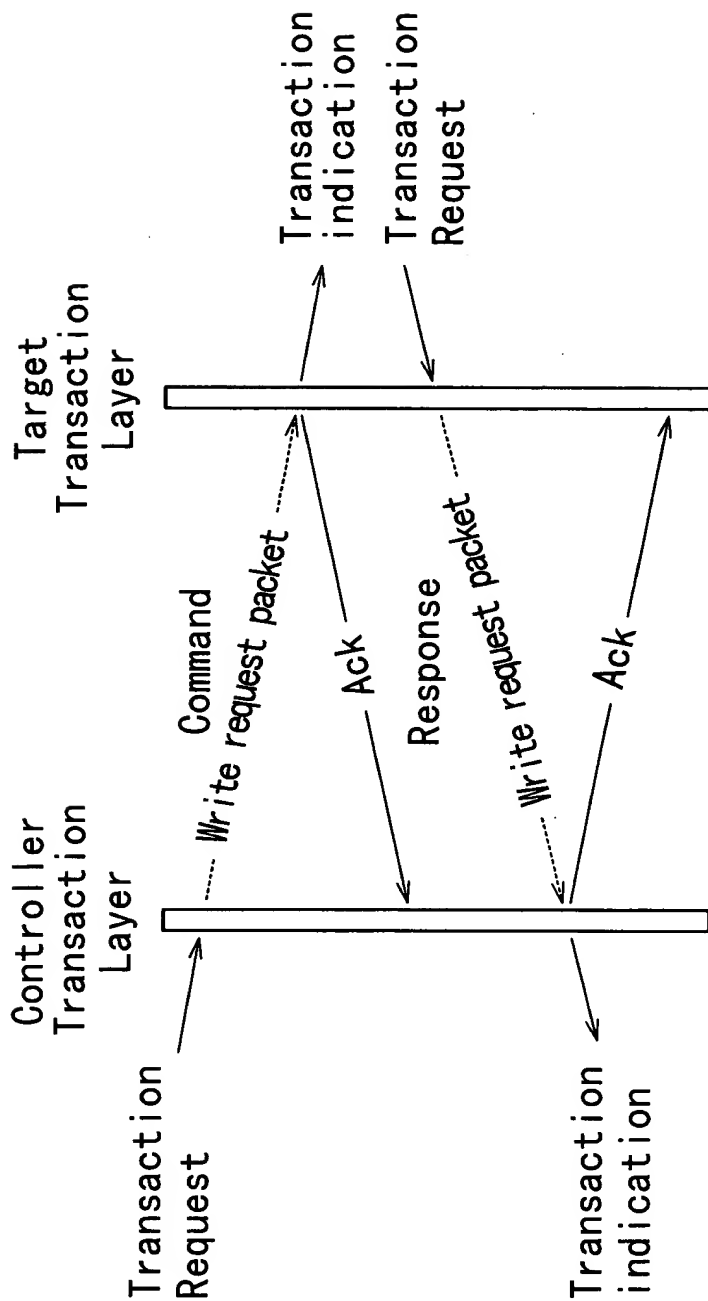


FIG. 24

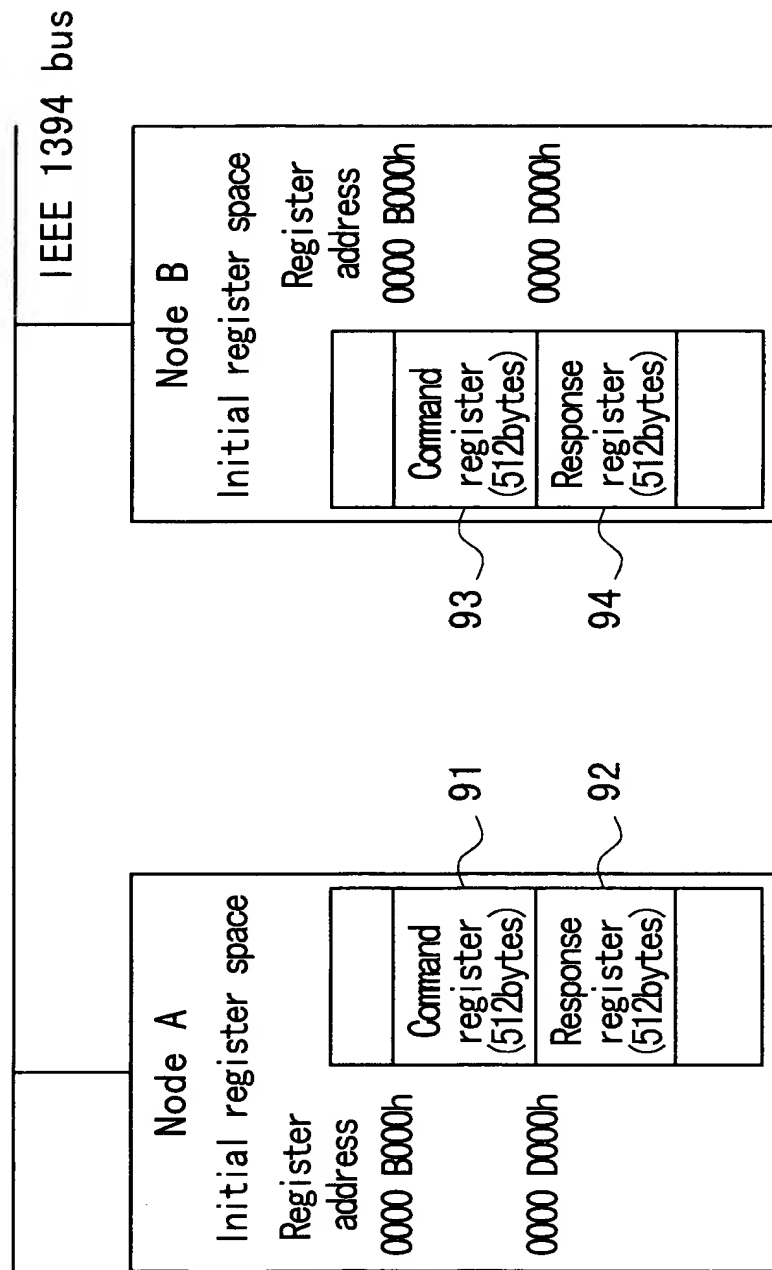
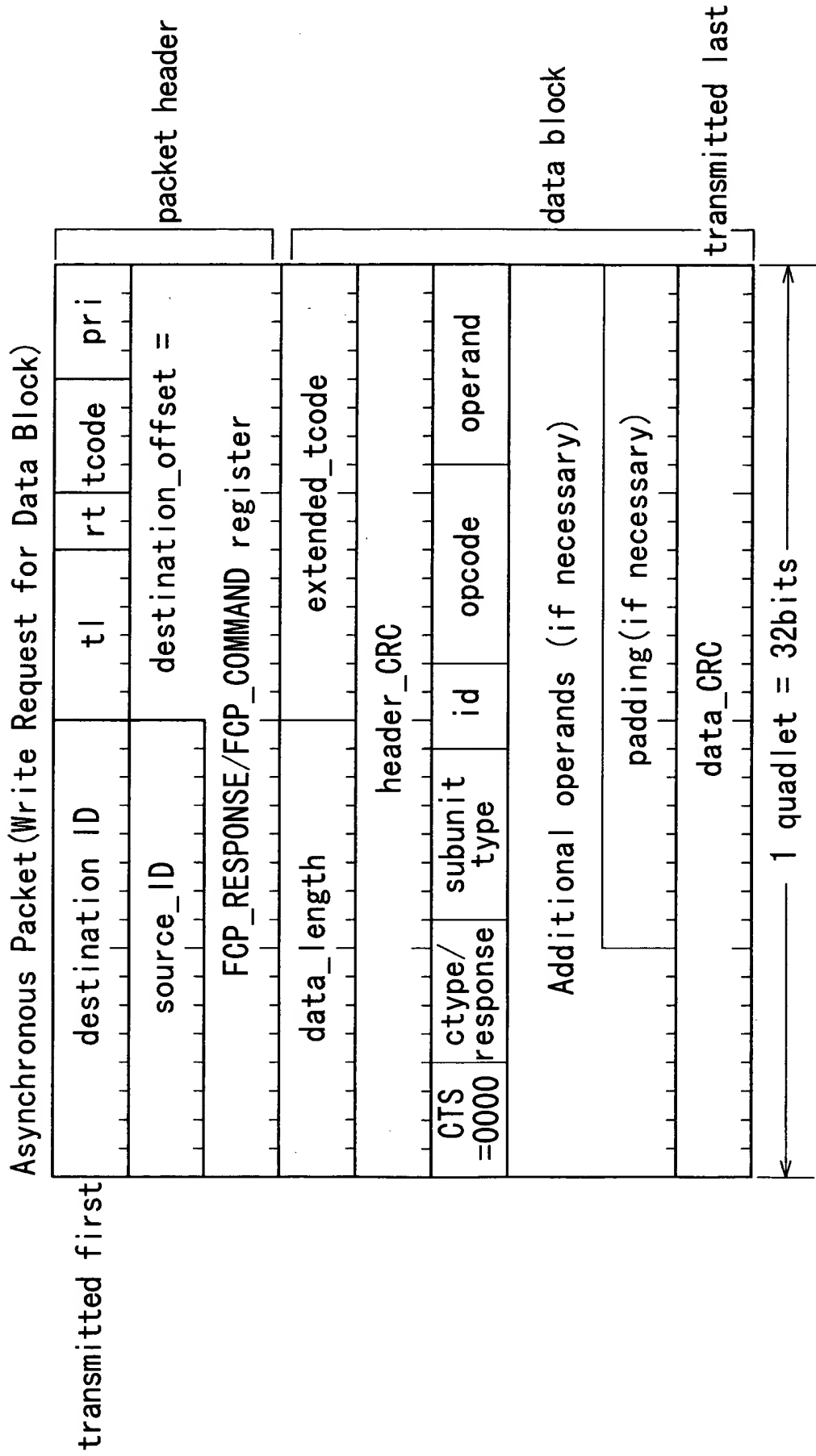


FIG. 25



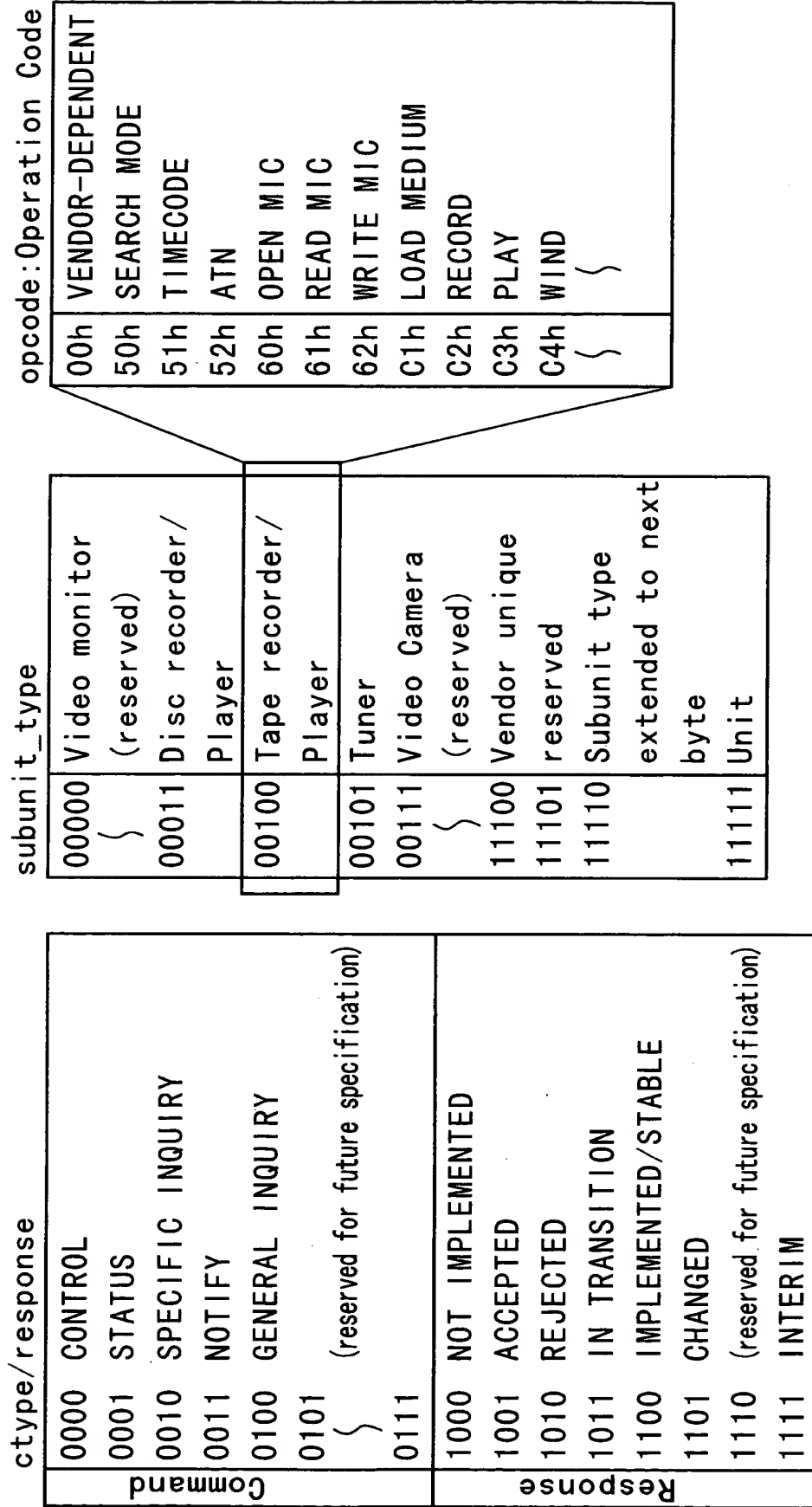


FIG. 26A

FIG. 26B

FIG. 26C

FIG. 27A

AV/C control		tape recorder IN THE CASE OF ID0			FORWARD
		/player	PLAY		
CTS= 0000	c type= 0000	subunit type= 00100	id= 000	opcode= C3h	operand= 75h

FIG. 27B

AV/C accepted		tape recorder IN THE CASE OF ID0			FORWARD
		/player	PLAY		
CTS= 0000	response =1001	subunit type= 00100	id= 000	opcode= C3h	operand= 75h

FIG. 28

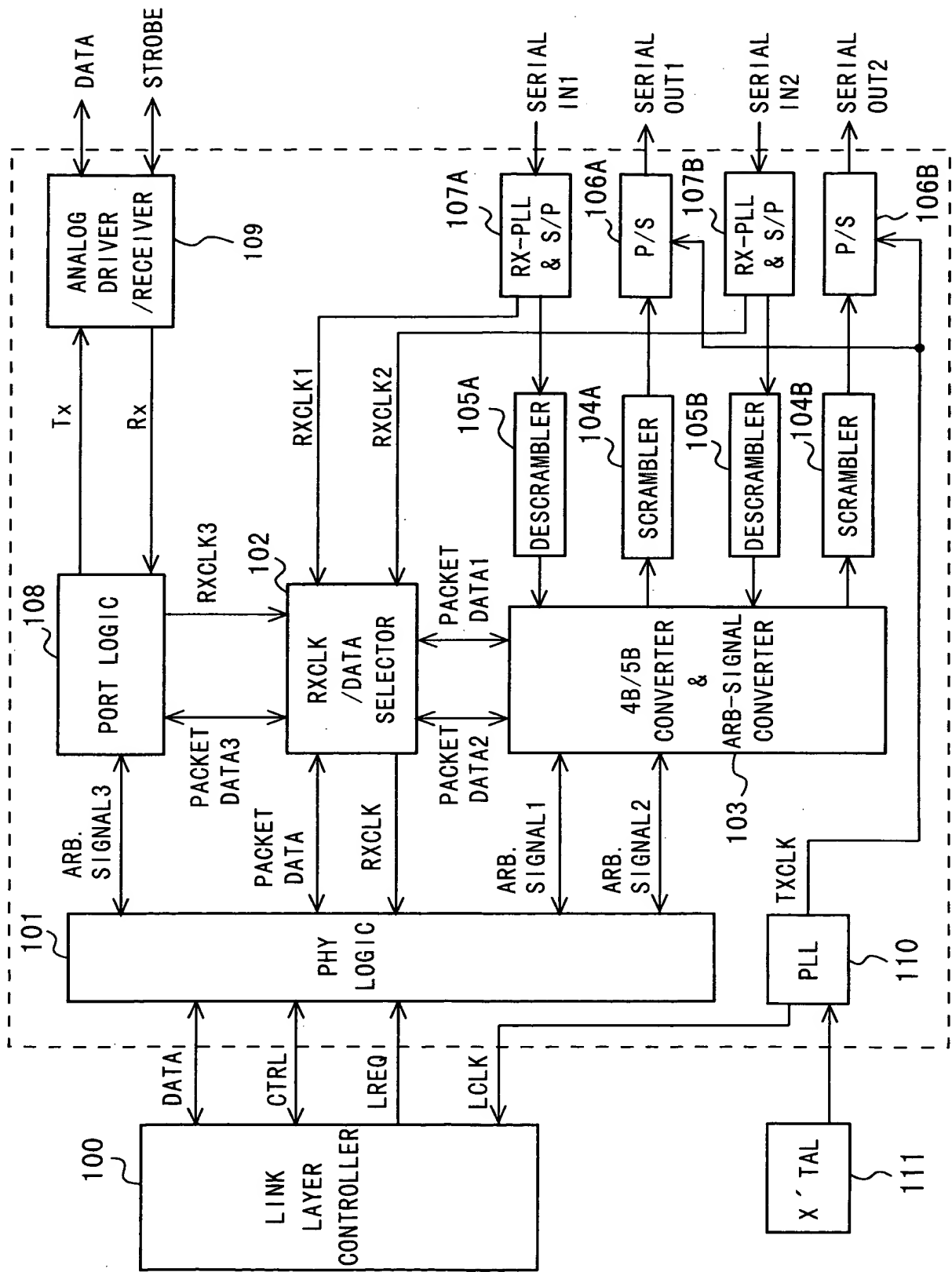




FIG. 30

